MIL-STD-1553 IP Cores –

An Emerging Technology

By

Marc Foster

Sealevel Systems, Inc.

And

Ofer Hofman and Duli Yariv

Sital Technology Ltd.

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Introduction

The MIL-STD-1553 serial data bus is widely used for control purposes in avionics, aircraft and space systems. Forty years since its release, 1553 is evolving from traditional integrated circuits (IC) to intellectual property (IP) cores integrated with Field Programmable Gate Array (FPGA) logic. The history of MIL-STD-1553, the advantages and requirements of 1553 IP cores compared to standard ICs, and IP core design best practices are discussed in this white paper.

History of MIL-STD-1553

MIL-STD-1553 was released in August 1973, and was first used in the F-16 fighter aircraft. At that time, a full 1553 Bus Controller (BC) or Remote Terminal (RT) design required three separate PCBs to accommodate the military grade TTL family components (54LSXX). Designs were usually based on micro code for control and state-of-the-art logic for designing the 1553 decoder.

Internally, units connected to the bus using transformers. Transceiver devices converted the analog signals to/from digital signals, and a digital controller converted the digital signals to/from Manchester code, managing the entire process of receiving and transmitting data in accordance with the 1553 specifications.

In the 80's and 90's, the first gate array ASICs (Application Specific Integrated Circuits) were produced offering a single chip that could handle the entire digital portion of the 1553 board. At the same time, the analog transceiver was also condensed from discrete devices into a single module, usually in a metal case and quite big.

The next step was for specialized companies such as DDC, Aeroflex NHi and others, to integrate the required digital and analog parts into a single module and produce 1553 ICs. Once introduced, these single mixed signal ICs dominated the market and today continue to represent the most common implementation of 1553.

IP cores, the latest emerging technology in MIL-STD-1553, integrate with other user logic into an FPGA that can be programmed to perform any digital circuit by means of loading the net-list of components.

Advantages of IP Cores

Combining an IP core with an FPGA to create an optimized 1553 solution is gaining widespread popularity with designers today. This approach offers numerous advantages over using traditional 1553 ICs including:

Reduced Cost

Assuming the FPGA already exists on a design, the price per 1553 node is only the cost of the analog transceiver and the IP core use-license. Since there are many suppliers for analog transceivers, pricing is competitive and including the use-license can deliver more than 50% cost reduction in 1553 node price for moderate quantities.

Easy Ability to Upgrade

Once a 1553 IC is soldered to a board the 1553 capabilities cannot be changed. Since FPGAs can be reprogrammed, the 1553 functionality can be enhanced, modified, or replaced by a new IP core if required. This architecture also allows configuration as various bus device configurations - such as one, two or more channels, or even different interface types such as WB-194 or H009, without any change in FPGA technology or PCB hardware. FPGAs can be reprogrammed in the field, via the 1553 bus in some cases, making upgrade simple.

Small Footprint Saves Board Space

Since an FPGA often already exists in a design for other tasks, adding an IP core may not require any additional ICs on the board. The IP core might consume 2 to 15% of a common FPGA, thus having a very small impact on its size. In this case, all that is needed on the board is the analog transceiver interfacing with the FPGA. The analog transceiver is much smaller than a dedicated 1553 IC and has fewer pins; therefore the required board space is reduced.

Smaller footprint and use of a single logic device for several channels also contributes to extending MTBF (Mean Time Between Failure), improving reliability.

Easy Evaluation before Committing

IP cores can dramatically reduce the complexity of hardware design. Using tools like ModelSim, the entire functionality can be evaluated and simulated before a single trace is routed for the PCB. Free IP core evaluations can be quickly supplied by IP vendors upon request. These samples may include a limited version of the core allowing 95% of the functions contained in the full core. The customer can check simulations, integrate the limited IP core, and test the behavior in the lab. No order or commitment is needed from the customer for the supply of the limited net-list, thus reducing risks, costs and design time.

Future-Proof Designs

IP cores are not FPGA specific and the core can be moved to a different FPGA part in the event of obsolescence. This compatibility allows users to update their board and FPGA technology while maintaining the proven core functionality.

Eliminate Problems Related to Single Source

Each 1553 IC has a unique interface and functionality. This fact makes it almost impossible to easily change the vendor for the parts since it would require a hardware and software redesign. Having a sole source raises price, availability, and obsolescence concerns.

An IP core implementation eliminates these problems. Once the IP core is licensed to a customer, the supply chain is simplified. The customer integrates the IP core in the form of EDIF net-list into the FPGA and procures the FPGA from a variety of distribution sources themselves, eliminating the dependence on the 1553 IC vendor.

Important Considerations in Choosing IP Cores

MIL-STD-1553 IP cores are available from several companies and, as you might expect, performance and quality can vary. To make sure you are choosing correctly, consider these important design considerations:

1553 Validation Testing

Like any other MIL-STD-1553 component, full 1553 validation testing is required to certify proper IP core compliance to 1553 electrical and software requirements. Choosing an IP core that has been approved through third-party testing will prevent surprises and delays later in the project.

Small Code Size

As discussed before, one of the advantages of IP cores over ICs is the fact that IP cores can reside within an FPGA that performs other functions as well. To allow room for this additional functionality while keeping FPGA cost reasonable, the IP core should require minimum FPGA resources.

Support for a Wide Range of FPGA Vendors and Families

IP cores should fit any FPGA vendor and family, with features ranging from general purpose to FPGAs with specific characteristics such as RAD-Hard, low power, non-volatile, and high memory volume. Customers can select the appropriate FPGA device based on these characteristics and IP vendors should be able to supply the appropriate net-lists for the parts. The VHDL source code from which the net-list produced should be vendor independent in code style to support all FPGA families.

Support for Any Clock Frequency

Multiple clock domains may cause overhead in FPGA design, or in some cases bad data read/write cycles. It is important, therefore, that the IP core support a clock frequency that is already available on the target board, such as PCI (33/66MHz), or PCI Express (125MHz).

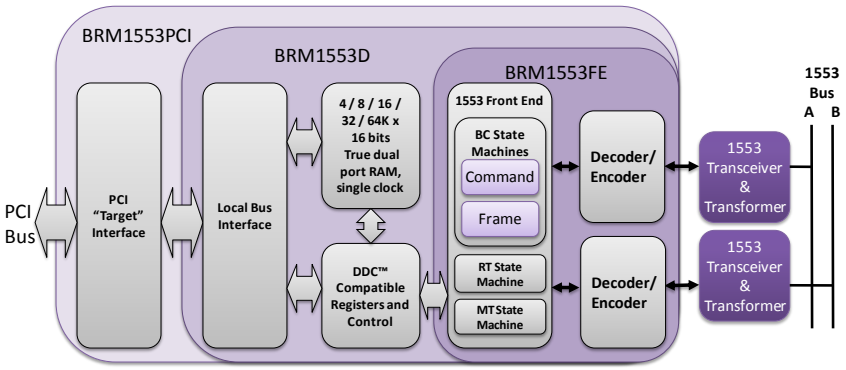
Compatibility with Legacy Software

Software integration is a critical aspect of migrating from an IC based design to an IP core. In most cases, engineers will not want to make changes to their existing working software environment. IP cores should be software compatible with legacy 1553 ICs, allowing the designer of a 1553 interface to replace an existing IC with an FPGA-based IP core with minimal risk.

Summary

IP cores offer many advantages over traditional 1553 ICs including lower cost, reduced size, easy ability to update, improved availability and lifecycle control. Combining the benefits of FPGAs and IP cores provides a small-size, robust, reliable, and future-proof solution for MIL-STD-1553 interface perfect for custom board implementations.

Sealevel Systems, Inc. has partnered with Sital Technology to supply MIL-STD-1553 IP core products engineered for military, aerospace, and avionics applications. Customers can choose between various available configurations and interfaces. From the very small and simple 1553 Front-End (FE), designed for simple applications where no CPU is controlling the system, to the most complex implementations, where a Local Bus is used by the CPU or where PCI bus is used (PCI).



The BRM1553FE core is suitable for simple 1553 applications, protocol translators and hardware based implementations. BRM1553D and BRM1553PCI are suitable for more complex 1553 implementations, where the application is controlled by software.

The BRM1553D and BRM1553PCI cores are software compatible to DDC® Mini-Ace® and Micro-Ace® components, allowing customers to re-use existing architectures and know-how.

All Sital IP cores work with any FPGA, clock frequency and 1553 transceiver, providing the user with the most robust, yet flexible, solution available. Each IP cores is third-party validation tested and offers software compatibility with existing ICs, perfect for retrofitting legacy applications. To learn more about our wide range of MIL-STD-1553 solutions visit http://www.sealevel.com/store/serial/mil-std-1553.html or call us today to discuss your specific requirements.

Contact Information

Marc Foster
Director of Strategic and Government Sales
Sealevel Systems, Inc.
2779 Greenville Highway
Liberty, SC, 29657
864-843-4343
www.sealevel.com
marcf@sealevel.com