# White Paper: Creative Custom Design Services Solve Problems

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## Introduction

Some of our favorite custom projects require solving problems by being creative and trying new things. The first step is always to carefully understand the problem, then formulate and test a prototype. Sometimes, a fundamental question needs to be answered before the real design work can begin. This white paper describes a real world example of this process.

## The Problem

A Sealevel customer required a very low power computer that could control application specific I/O and be installed outdoors. To reduce design time and risk, we chose a computer on module (COM) architecture using a SMARC (Smart Mobility ARChitecture) computer module and developed a custom carrier board for the I/O, power circuit, and connectors. In this case, the SMARC module was a low power Atom design from ADLINK.

To protect the electronics from the environment, we decided to encapsulate the entire circuit assembly in a non-conductive potting material. It seemed like a good approach, but a question lingered: would the potting material affect the operation of the electronics.

Two distinct risks were identified. First, would the potting material flow into the connector and cause the electrical connection to be either partially or fully lost after curing? Second, would the mere presence of the potting material disturb the signal integrity of high-speed signals?

There was only one way to know – try it and test everything.

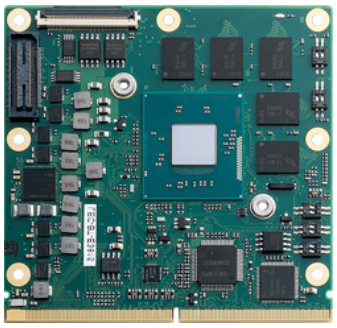

**Figure 1. ADLINK SMARC module with Atom processor**

## Procedure

SMARC CPU modules use plated MXM3 (Mobile PCI Express Modules) card edge connectors with gold fingers on both the top and bottom surface of the board. The SMARC module mates to the Sealevel custom carrier board using a connector that is similar to SODIMM RAM module connectors used in laptops and embedded computers.

To test the interaction of the SMARC connector with the potting material, our carrier board was designed to allow a high-speed differential signal to be injected into the board through a pair of SMA connectors. These signals then travel through the SMARC connector, through a small loopback board, back through the SMARC connector and exit the carrier board through another pair of SMA connectors located adjacent to the input pair. The traces are routed through the carrier as matched 100 ohm differential impedance pairs. This design was duplicated using a total of 77 sets of connectors in order to test each of the signal pins on the SMARC connector and also identify any changes in behavior related to routing or signal length.

Sealevel engineers then used the in-house 3D printer to make a fixture with a hollow reservoir to hold the carrier board and encase the SMARC module within the potting material.


**Figure 2. Carrier board and SMARC loopback board**


Figure 3. Carrier board with SMA test connectors and SMARC loopback installed.

## Test Method

A square wave signal was created by a Tektronix AWG7122C function generator, injected into the test board. The output of the test board was captured and analyzed by a Tektronix MSO71254C mixed signal oscilloscope. The test signal generated was 2.5GHz, 1V peak-peak to make it similar to the PCI Express 2.0 specification, which is the fastest signaling supported by the target SMARC module.

The test signal was injected into each signal path and the output waveform analyzed, recorded and a custom "eye mask" fitted to each path. To fit the mask to the signals, the average peak positive and negative differential voltages were recorded and the eye mask limits were set 75mV above and below these levels. This very narrow margin was chosen to highlight small changes in the signal levels before and after potting.

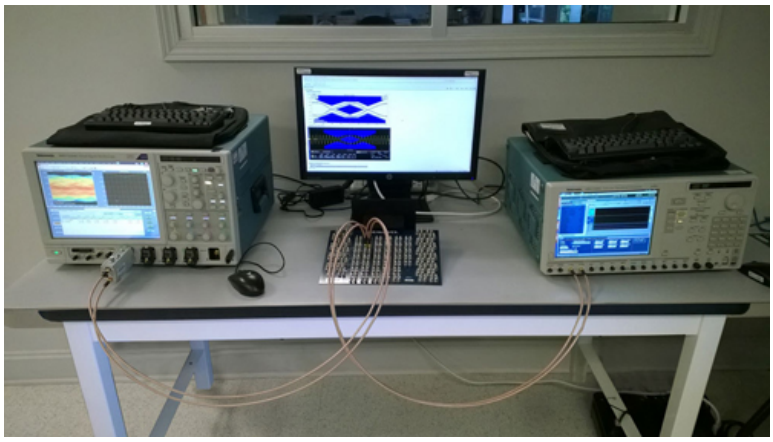

Figure 4. Full test setup with high speed Tektronix oscilloscopes.

After each signal path had been characterized, the SMARC connector and loopback board were fully potted.

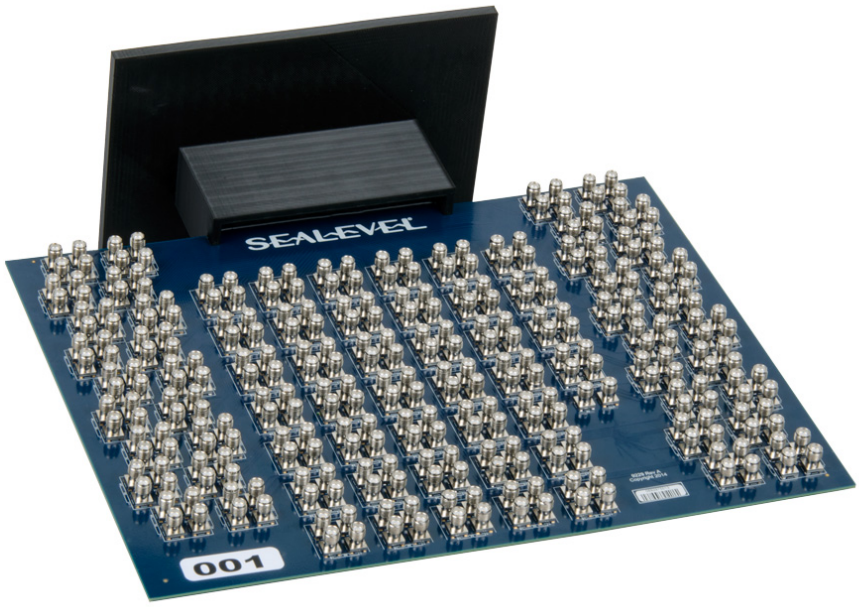


**Figure 5. Carrier board mounted in test fixture with potting material applied.**

After the potting material had cured for 24 hours, the signal paths were analyzed to determine if electrical continuity was lost or if high-speed signal integrity was affected.

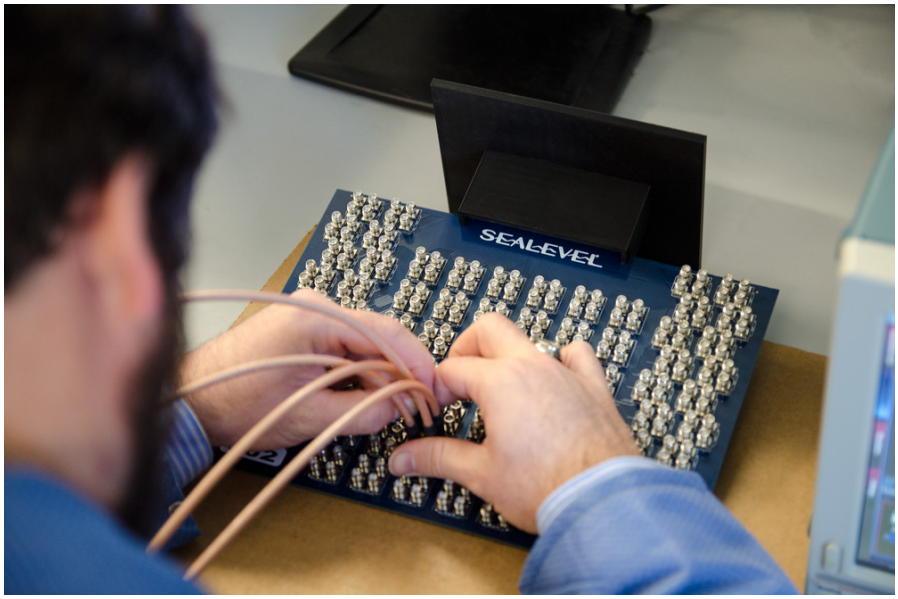


Figure 6. Sealevel engineer performs signal testing.

## Results

Of the 310 individual signal paths tested, continuity was not lost on any signal path. A minor change was observed after the connector was potted, however, the change was small enough to not likely cause compliance problems on the high-speed signals in the PCI Express Rev 2.0 speed range.

Figure 7 shows the test report for the signal trace marked by connector P1 prior to potting. Note that the average peak-peak voltage of the eye opening was 418.6mv- (-436.4mV) = 855mV. After potting the eye opening was reduced to 707mV (figure 8).

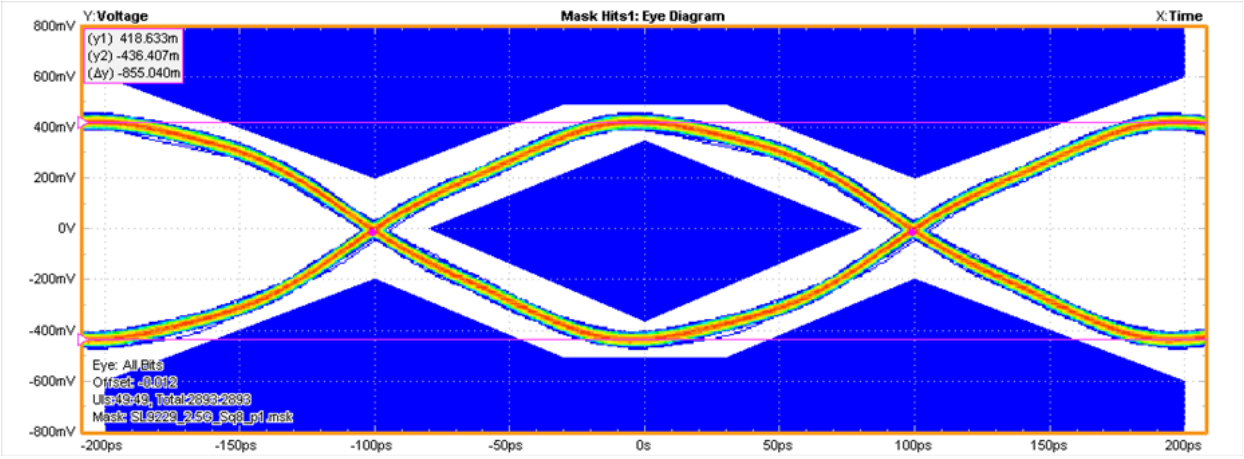


Figure 7. Eye diagram before potting

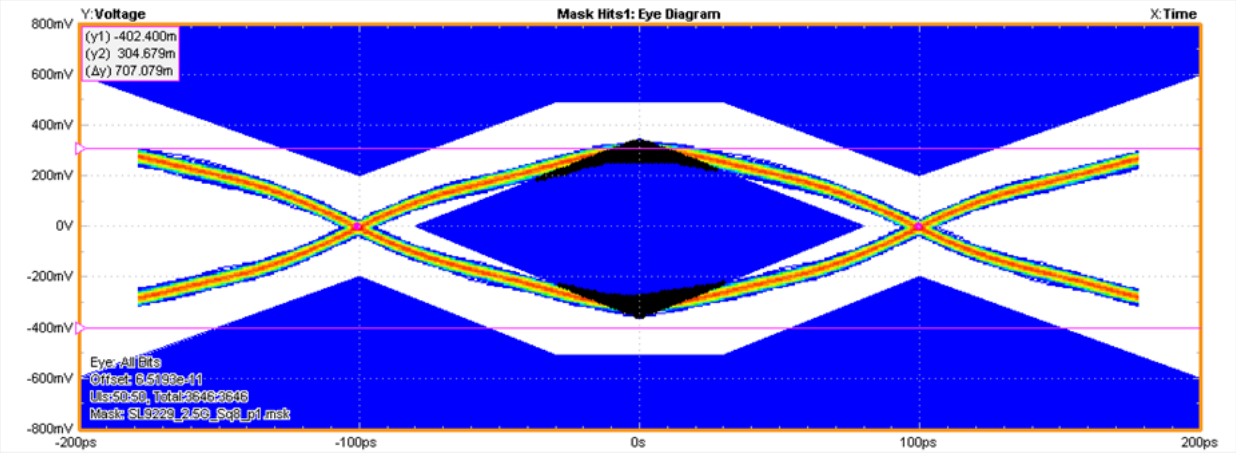


**Figure 8. Eye diagram after potting shows a slight degradation in differential signal.**

Some signal paths had different baseline characterizations due to the orientation and length of the traces on the carrier board test fixture. Figure 9 shows the worst-case scenario eye mask. The pair identified as P309 had a baseline average differential voltage of 291mV. After potting this eye actually improved with a measured opening of 315mV (figure 10).

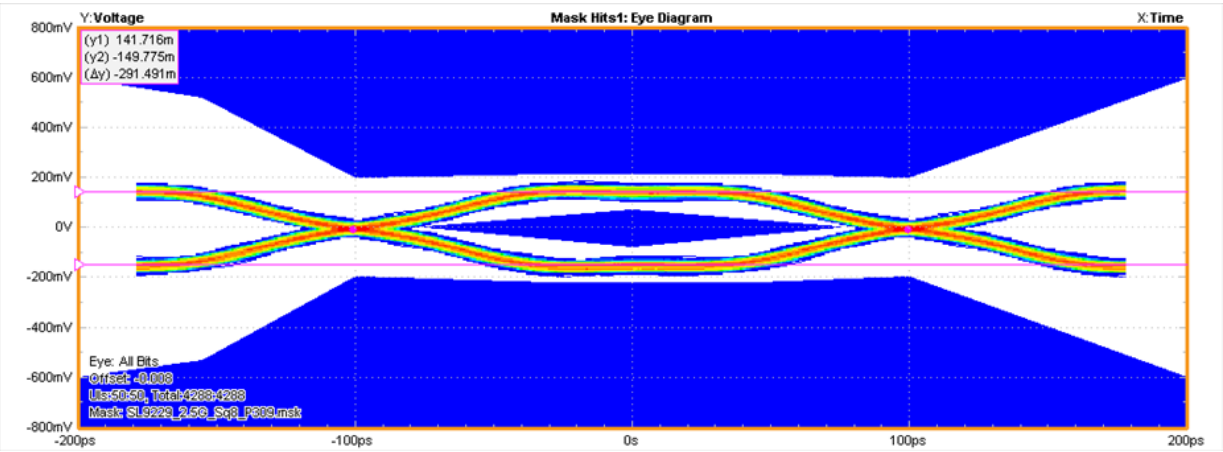


**Figure 9. Eye mask diagram before potting.**

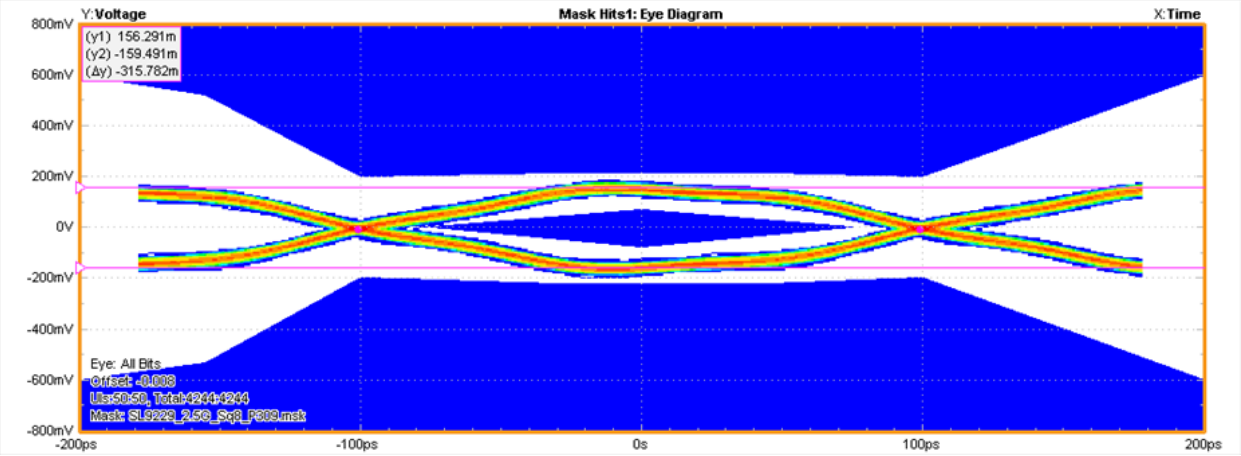


**Figure 10. Eye mask diagram after potting actually shows improvement.**

The application of the potting caused the peak differential voltage to increase on some channels while it was reduced on others. The average absolute change across all channels sampled was 10%.

P309 had the worst overall baseline signal attenuation due to its long total trace length. The test signal was applied to this signal path and the standard “PCIe 2.0 RX Eye Mask” was applied. The signal and mask are shown in Figure 11. The resulting test signals still fits well within the mask template even after the application of the potting material.

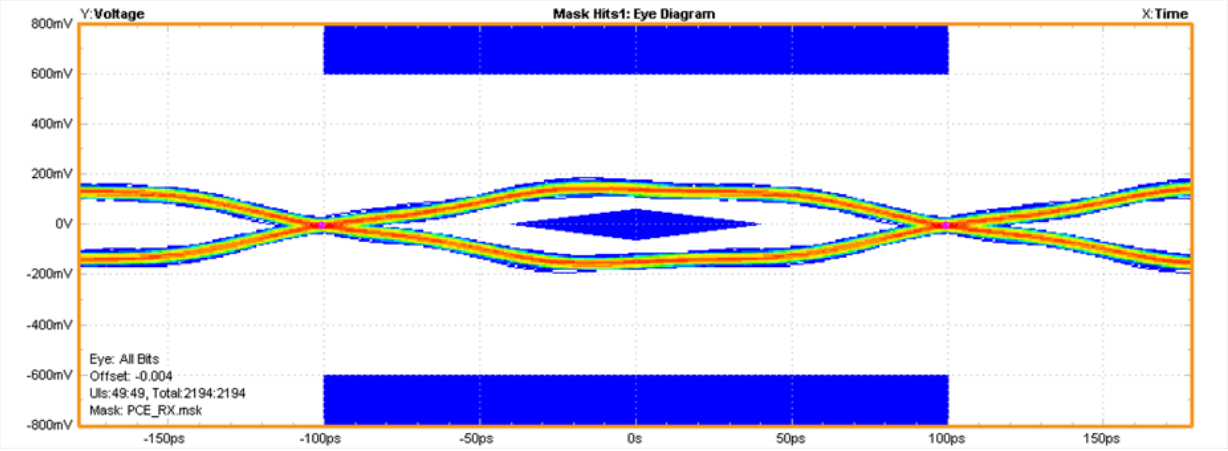


**Figure 11. Worst performing signal pair still meets PCIe 2.0 eye diagram requirements with margin to spare.**

## Other Considerations

This test was designed to test the signal integrity changes caused by the presence of the potting material in and around the SMARC connector. Two details should be considered that can also affect signaling.

1. Many of the trace lengths were in excess of that allowed by the SMARC specification. This is due to the amount of paths tested and the space required to accommodate the test connectors. The longest signal path was over 26 inches, while the signal lengths allowed by the SMARC specification for high-speed interfaces are much shorter. The PCIe 2.0 specification limits traces to 12 inches.
2. In the test setup, each signal path was routed through the SMARC connector interface twice. In an actual carrier board application, each high-speed interface path will originate on the SMARC module and terminate on the carrier board, passing through the SMARC connector only once.

Because of these two factors, the test conducted represents a worst-case scenario and actual signal integrity in the target application will be much less susceptible to disturbance on an actual SMARC module and carrier board.

## Conclusion

From the empirical data gathered during testing, we demonstrated that applying a potting compound to protect a SMARC module and carrier board was a viable option. Although some differences in signaling were measured after potting, the results were small and inconsistent. As a result of this testing, we were confident proceeding with the design of the actual application specific carrier board required for the customer's application.

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