White Paper: Using FPGAs to Improve Embedded Designs

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Introduction

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are programmed after manufacturing to accomplish application specific functionality. FPGAs experienced rapid technology advancement in the 1990s, and today are found in a vast variety of products ranging from simple consumer items to highly complex military systems.

The heart of the FPGA concept is programmability. This capability provides a virtually limitless choice of possibilities to designers for implementing circuits that would otherwise require many discrete components. The result is a more capable and adaptable design, reduced PCB size, and reduced cost.

In this white paper, we look at the variety of ways FPGAs are used in Sealevel embedded designs.

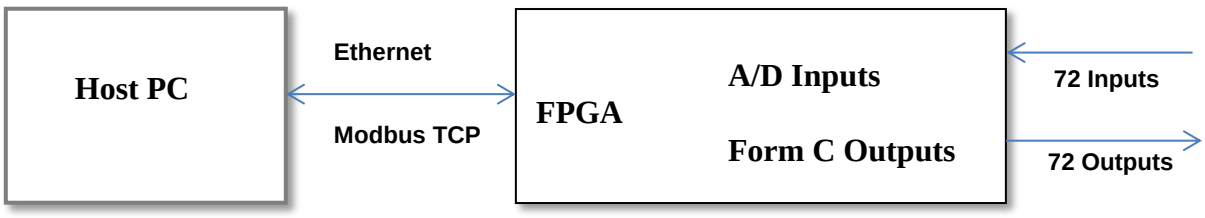
Building a CPU and Application Specific Logic with FPGAs

To run an operating system and execute an application program written in a high-level language requires a discrete processor or microcontroller, right? Not anymore – the core CPU functionality can be designed into a FPGA along with application specific circuitry to create an optimized embedded system. Sealevel recently utilized this architecture in the design of a custom remote monitoring and control appliance that is part of a maritime navigation control system.

Overview

Sealevel's customer required an I/O controller that could constantly monitor the values of 72 analog inputs, each ranging ±53 VDC, and immediately report change of state information to a host computer over an Ethernet Modbus TCP communications link. The host would then make a determination of the necessary actions required and issue appropriate commands to the I/O controller to activate one or more of 72 Form C relay outputs.

Figure 1. I/O Controller Hardware Architecture



Design Architecture

Constantly monitoring the analog inputs and reporting change of state removes the overhead of polling the I/O from the host processor, but requires intelligence be built into the I/O controller. Sealevel chose the NIOS II "soft processor" from Altera for integration into the FPGA for flexibility, tight integration with the FPGA logic, and the ability to create custom I/O peripherals. The FPGA also incorporates a 10/100/1000 Ethernet MAC core that interfaces directly to the NIOS II processor, and connects to the host via external PHY.

The NIOS II core resides in the FPGA fabric and provides a full 32-bit processing engine capable of running an operating system and allowing application software to be developed in a high level language. Sealevel selected and customized µClinux for the OS and C# for the programming language. External Flash memory is used to load the OS and application program, and both the OS and the application run from DDR2 memory. A robust Ethernet stack is included in the µClinux kernel. Interface logic for controlling the 72 inputs and 72 outputs is also built into the FPGA along with the processor subsystem, making a powerful, compact, and cost efficient solution.

Using a FPGA to Simplify COM Express Designs

FPGAs are a great way to extend system I/O in a processor subsystem. An example can be found in a recent Sealevel custom COM Express computer design used as part of an emergency communications system.

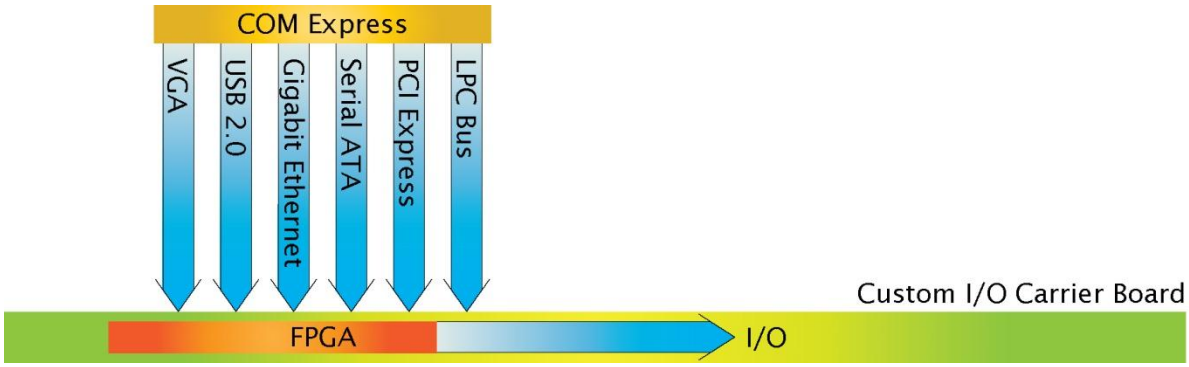
Overview

Sealevel COM Express systems combine an off-the-shelf Computer on Module (COM) containing the functionality common to most systems (processor, memory, graphics, USB, Ethernet, SATA) with a Sealevel-designed custom carrier board that includes application specific I/O and interface connectors. This combination provides the benefits of a full custom design while reducing the time, costs, and design risks. In this application, a FPGA was used to interface a custom carrier board with 256 analog and digital I/O to the COM Express CPU module using a PCI Express (PCIe) interface.

Design Architecture

The signals necessary to interface the I/O are brought down from the COM Express board via mating connectors, and the carrier board's functionality and mechanical footprint are designed to best fit the application.

Figure 2. COM Express Interface to Custom Carrier Board



A FPGA is the perfect solution for interfacing a high-speed PCIe lane from the COM Express module to the I/O on the carrier board. Sealevel engineering created a PCIe endpoint and custom I/O interface logic in FPGA that allows the application running on the COM Express module to easily read and write data using a memory mapped addressing format. The result is an elegant software interface and fast system I/O response time.

Interface Conversion for Tactical Military Communications

Marrying dissimilar communication interfaces is a dilemma in many applications. Often legacy electronic equipment needs to be used with modern computers that do not support the interface or protocol for the device. This requirement seems especially true for military systems where it is frequently necessary to connect older infrastructure equipment such as radars and radio systems to new systems.

Overcoming this challenge is simplified through the use of FPGA technology as demonstrated by a custom USB to synchronous data cable designed for the U.S. military that meets the core application requirements for fast throughput, low power, and small, rugged mechanical design.

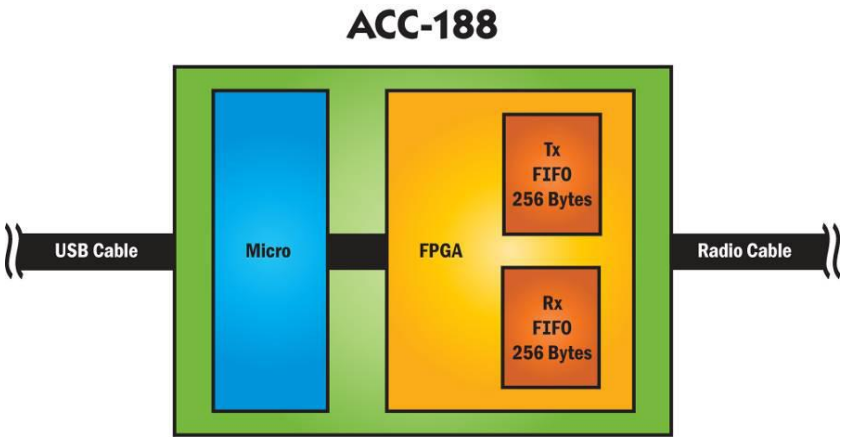
Overview

Unfortunately, the vast majority of the tactical data communications and situational awareness systems currently in use by the military are comprised of various makes and models of older vintage tactical radios, making it difficult to achieve interoperability at the theater level. To solve this problem, Sealevel worked with the Defense Information Systems Agency (DISA) to develop the ACC-188, a non-proprietary, interoperable USB synchronous interface that works seamlessly with the PDA-184 tactical data communications software application developed by DISA. The ACC-188 adapter and PDA software enable PC compatible computers (mainly laptops) to connect to tactical radios to transmit and receive IP data such as email, text messages, GPS maps, images, coordinates, and other communications.

Design Architecture

The heart of the design is an 8-bit microcontroller with integrated USB port and a FPGA. The FPGA design includes a 256-byte input FIFO for receiving high-speed serial data from the radio. Using the clock signal supplied by the radio, the incoming data is clocked into the FIFO and stored until the microprocessor organizes the data into byte format and transfers the formatted data to the PC via USB packets. Similarly, on message transmission, the USB packets are sent to the Transmit FIFO and subsequently clocked out one bit at a time to the radio.

Figure 3. ACC-188 Hardware Architecture.



The FPGA also helps to reduce the power required by the ACC-188. Considering that the USB port on the host computer fully powers the ACC-188, the design is optimized to consume less than 0.3 watts of power to minimize battery drain when used with laptops operating on battery. Power is a huge consideration since there is often no AC power source available in combat situations.

Figure 4. Sealevel's 9065 USB to Synchronous Cable Adapter.

Summary

FPGAs have become a key technology for modern electronic design. The very nature of a FPGA-based design affords extreme flexibility that, when used properly, can solve a huge array of problems while saving time, board space, and cost.

Traditionally, FPGAs are extremely useful in interfacing disparate system components by performing data manipulation or timing conversions. Incorporating both hard and soft IP cores further expands the reach and effectiveness of FPGA designs to the point that even complex functionality can be implemented without the need for a separate discrete processor or interface device. The exciting advancements in FPGAs have occurred over a relatively short period of time, and there is every reason to believe that improvements will continue that make FPGA design an indispensable part of a designer's repertoire.